Remarks

This is in response to the Office Action dated April 1, 2005.

Per the above amendment, claims 1-4 have been amended and new claims 5-7 added. In addition, the specification has been amended at those sections pointed out and objected to by the examiner on page 5 of the Office Action.

Hereinbelow applicant traverses the objections and rejections by the examiner.

Objection to Drawings and Rejection of Claims under 35 U.S.C. I12

The drawings were objected to and claims 1-2 were rejected under 35 USC 112, 1st paragraph as being non-enabling.

35 USC 112, 6th paragraph states: "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof."

It is respectfully submitted that every "means" and "steps" recited in the pending claims has clear ample support in the specification.

To wit, claims 1 and 3 are supported by the embodiment of Fig. 2; whereas claims 2 and 4 are supported by the embodiment of Fig. 5.

Each objection raised by the examiner is particularly responded to per the following.

In claims 1 and 3: the examiner objects to " **means for** getting information about a frame pixel number of the incoming bit stream":

According to the specification, page 10, lines 20-23, the size of every picture (frame) means the number of pixels composing every picture. Page 11, lines 8-11, of the specification reads as follows: "The demultiplexer 12 separates the input signal into the picture representing data and the picture-size-related information. Thus, the demultiplexer 12 extracts the picture-size-related information from the input signal."

Therefore, the function of "getting information about a frame pixel number of the incoming bit stream" is implemented by the demultiplexer 12, or its equivalent, per shown in Fig. 2.

In claims 1 and 3: the examiner also objects to the following means plus function language: " setting a decoding picture rate of a moving picture from a relation between the frame pixel number and a decoding processing capability".

Page 11, lines 19-22, of the specification reads as follows: "The picture rate setting device 13 determines a desired decoding picture rate in response to the decoding capability value and the picture size represented by the picture-size-related information."

Therefore, the function of "setting a decoding picture rate of a moving picture from a relation between the frame pixel number and a decoding processing capability" is implemented by the picture rate setting device 13, or its equivalent, as shown in Fig. 2.

In claims 1 and 3, the examiner objects to "**means for** causing at least a portion of bidirectional inter-picture prediction pictures in the incoming bit stream to be not decoded, and performing decoding of the incoming bit stream at the decoding picture rate to get decoded pictures".

According to the specification, page 14, line 12 to page 15, line 8, the switch 8 separates portions of the picture-representing data into discarded ones and non-discarded ones in response to the picture rate signal, and portions of the picture-representing data which represent B pictures (bidirectional inter-picture prediction pictures) can be selected by the switch 8 as discarded ones. Only the non-discarded portions of the picture-representing data are transmitted from the switch 8 to the variable length decoder 1 before being decoded by the variable length decoder 1. On the other hand, the discarded portions of the picture-representing data are not transmitted from the switch 8 to the variable length decoder 1, and are not decoded.

Therefore, the functions of "causing at least a portion of bidirectional inter-picture prediction pictures in the incoming bit stream to be not decoded, and performing decoding of the incoming bit stream at the decoding picture rate to get decoded pictures" may be implemented by the combination of the switch 8, the variable length decoder 1, and the subsequent devices 2. 3, 4, 5, 6, 9, and 10 which are shown in Fig. 2.

In claims 1 and 3, the examiner objects to "**means for** interpolating a picture of the previously-mentioned decoded pictures to get a reproduced picture at a prescribed picture rate".

According to page 19, line 22 to page 20, line 5 of the specification, the frame memories 5 and 10 are responsive to the picture-rate signal. In the case where portions of the picture-representing data are discarded by the switch 8, the frame memory 5 or 10 repetitively outputs the same picture signal to the switch 6 a given number of times to implement interpolation for frames corresponding to the discarded portions of the picture-representing data. As a result, the second reproduced signal generated by the switch 6 has a prescribed picture rate.

Therefore, the function of "interpolating a picture of the previously-mentioned decoded pictures to get a reproduced picture at a prescribed picture rate" is implemented by the frame memories 5 and 10, and the switch 6, which are shown in Fig. 2.

In claims 2 and 4, the examiner objects to "**means for** getting information about a frame pixel number of the incoming bit stream, and setting a decoding method not decoding all bidirectional inter-picture prediction pictures in the incoming bit stream in cases where decoding of bidirectional inter-picture prediction pictures in the incoming bit stream can not be done from a relation between the frame pixel number and a capacity of a frame memory for decoding."

Similar to the above discussion relating to claims 1 and 3, the function of "getting information about a frame pixel number of the incoming bit stream" is implemented by the demultiplexer 12 which is shown in Fig. 5.

According to page 24, line 10 to page 25, line 6 of the specification, when the switch 8A discards B pictures, the decoding by the variable length decoder 1, and the later devices does not decode all B pictures. Page 23, lines 3-6 of the specification reads as follows: "The decoding method setting device 23 determines a desired decoding method in response to the picture size represented by the picture-size-related information and the preset capacity of the frame memories 21 and 22."

Therefore, the function of "setting a decoding method not decoding all bidirectional inter-picture prediction pictures in the incoming bit stream in cases where decoding of bidirectional inter-picture prediction pictures in the incoming bit stream can not be done from a relation between the frame pixel number and a capacity of a frame memory for decoding" is implemented by the decoding-method setting device 23 and the switch 8A.

In claims 2 and 4, the examiner objects to " **means for** decoding the incoming bit stream in accordance with the previously-mentioned decoding method to get decoded pictures."

In the embodiment of Fig. 5, the signal portions selected by the switch 8A are decoded by the run length decoder 1 and the subsequent devices 2, 3, 4, 6. 9, 21, and 22 in the decoding method decided by the decoding-method setting device 23 (see the specification, page 27. line 4 to page 26, line 6).

Therefore, the function of "decoding the incoming bit stream in accordance with the previously-mentioned decoding method to get decoded pictures" is implemented by the run length decoder 1 and the subsequent devices 2, 3, 4, 6, 9, 21, and 22 which are shown in Fig. 5.

In claims 2 and 4, the examiner objects to "a frame memory for decoding which uses a memory corresponding to 4 frames when bidirectional prediction is done as a memory corresponding to two frames double In pixel number in cases where bidirectional prediction is not done in accordance with the previously-mentioned decoding method, and getting a prescribed reproduced picture from the previously-mentioned decoded pictures":

The frame memory in claims 2 and 4 has support in page 25, line 7 to page 28, line 22 of the specification, and corresponds to the frame memories 21 and 22 which are shown in Fig. 5.

As for the "method" objections and rejections, the examiner is respectfully directed to the above noted portions of the specification which clearly provide the support for the methods as set forth in claims 3 and 4. And the attention of the examiner is again directed to 35 USC 112, 6th paragraph, which clearly allows the applicant to express the elements disclosed in the specification as "a means or step for performing a specified function".

As the specification, including the drawings as filed, clearly provide support for the means and steps as recited in the pending claims, it is respectfully submitted that there is nothing amiss about the drawings and that the rejection of claims 1 and 2 under 35 USC 112, 1st paragraph is without merit and should be withdrawn.

The rejection of claims 2 and 4 under the 35 USC 112, 2nd paragraph is believed to have been overcome by the amendment to those claims.

Art Rejection

Claims 1 and 3 were rejected under 35 USC 103 (a) as being unpatentable over Park (USP 6754274) and further in view of Mishima (USP 6549717) ; and claims 2 ad 4 were rejected under 35 USC 103 (a) as being unpatentable over Park and further in view of Kurihara (USP 5841475).

The first feature of the inventions of claims 1 and 3 is that the decoding picture rate is set in response to the frame pixel number, that is, the frame picture resolution. The second feature of the inventions of claims 1 and 3 is that B pictures are not decoded to implement the decoding at the decoding picture rate, and the B pictures are reproduced by interpolation.

It is respectfully submitted that none of Park (USP 6754274), Mishima (USP 6549717), and Kurihara (US 5841475) teaches the first and second features of the inventions of claims I and 3.

The first feature of the inventions of claims 2 and 4 is that the decoding of B pictures is suspended in response to the frame pixel number, that is, the frame picture resolution. The second feature of the inventions of claims 2 and 4 is that a frame memory is used as either a 4-frame memory or a 2-frame memory depending on whether or not the decoding of B pictures is suspended.

It is respectfully submitted that none of Park, Mishima, and Kurihara teaches the first and second features of the inventions of claims 2 and 4.

The subject matters of new claims 5-7 are similar to or narrower than those of claims 1-4.

The apparatus of Park (US 6754274) does not decimate or thin some of pictures in response to the decoding capability or the picture resolution. As recognized by the Examiner, the apparatus of Park does not implement interpolation to generate pictures corresponding to discarded ones.

The Examiner alleges that Park, Fig. 4, block 10 and Fig, 5, block 201, column 5, lines 4-8, discloses setting a decoding picture rate from a relation between the frame pixel number and a decoding processing capability.

But a conventional reading of those portions of Park shows that Park merely teaches that information such as a picture size and a picture rate is obtained by analyzing a sequence header. Obtaining information about a picture size and a picture rate is completely different from setting a decoding picture rate from a relation between the frame pixel number and a decoding processing capability,

The Examiner states that Park, Fig. 4, block 10, Fig. 5, blocks 205 and 208, column 5, lines 17-25 and 35-39, disclose causing at least a portion of bidirectional inter-picture prediction pictures in the incoming bit stream to be not decoded.

It is respectfully submitted that those portions of Park in actuality disclose that B pictures are skipped during the high-speed reproduction and are not skipped during other-speed reproduction. Thus, the portions of Park referenced by the examiner do not teach skipping B pictures in response to the frame pixel number.

As pointed out by the Examiner, Mishima (column 36, lines 46-54) discloses that in the cases where the whole I picture and the whole P picture can not be read because of time limit, the data of the preceding screen is interpolated to allow output of the playback picture. As recognized by the Examiner, Mishima does not teach setting the decoding picture rate in response to the frame pixel number and suspending the decoding of B pictures in response to the frame pixel number.

Kurihara (column 8, lines 44-45) discloses that each of the memories 27 and 28 has a capacity which retains picture element data of a single block line. A single block line is different from one frame. Kurihara (column 9, lines 55-56, column 10, lines 9-11, and column 10, lines 50-52) suggests that each of the frame memories 11 and 12 has a capacity corresponding to one frame. Accordingly, Kurihara does not teach a frame memory usable as a 4-frame memory.

As recognized by the Examiner, Kurihara does not teach setting the decoding picture rate in response to the frame pixel number and suspending the decoding of B pictures in response to the frame pixel number.

The inventions of claims 1-4 are advantageous over the apparatuses of Park, Mishima, and Kurihara in that the decoding of an MPEG bit stream is properly implemented depending on the picture resolution, and reproduced pictures are reliably obtained without the occurrence of the bankruptcy of the decoding.

In light of the above, it is respectfully submitted that the claimed inventions are patentably distinguishable over the prior art. Accordingly, the examiner is respectfully requested to reconsider the application and pass the same to issue at an early date.

Respectfully submitted,

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